FIG. 1

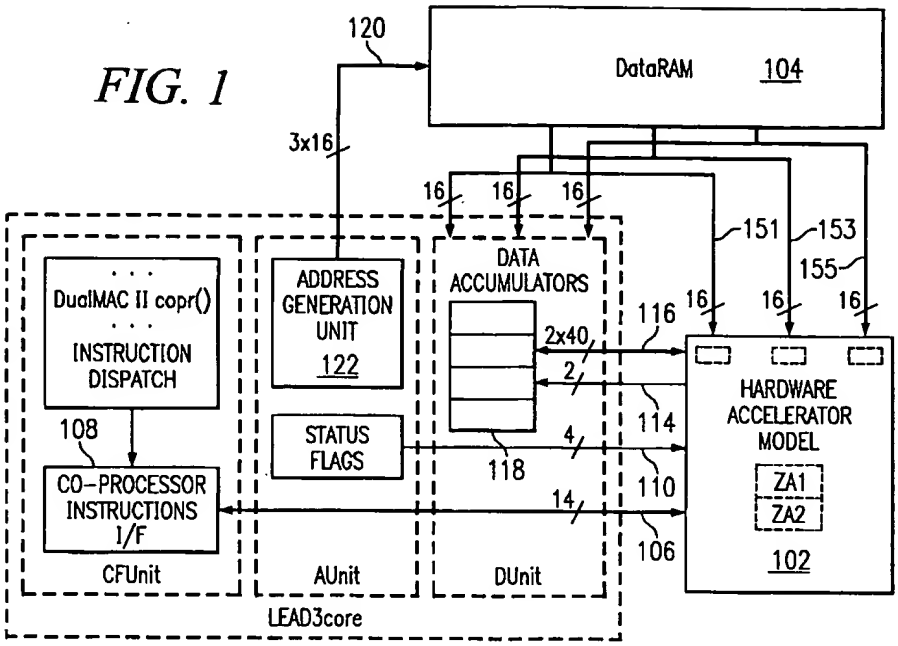


FIG. 2

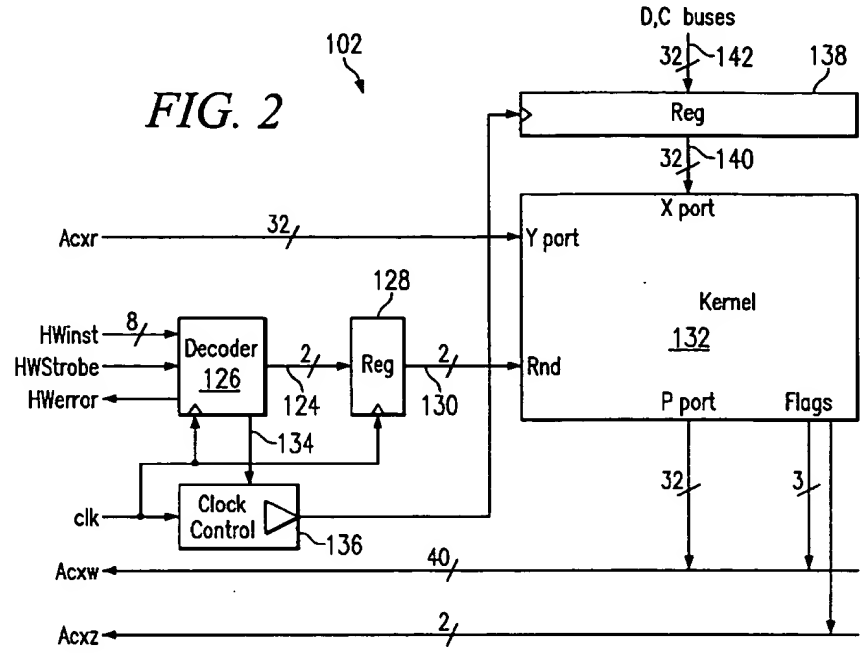

102
D,C buses
32
142
138
Reg
32
140
X port
Acxr
32
Y port
128
Kernel
HWinst
8
Decoder
126
2
Reg
2
132
HWStrobe
Rnd
HWerror
124
130
P port
Flags
134
32
3
clk
Clock
Control
136
40
Acxw
2
Acxz

FIG. 3

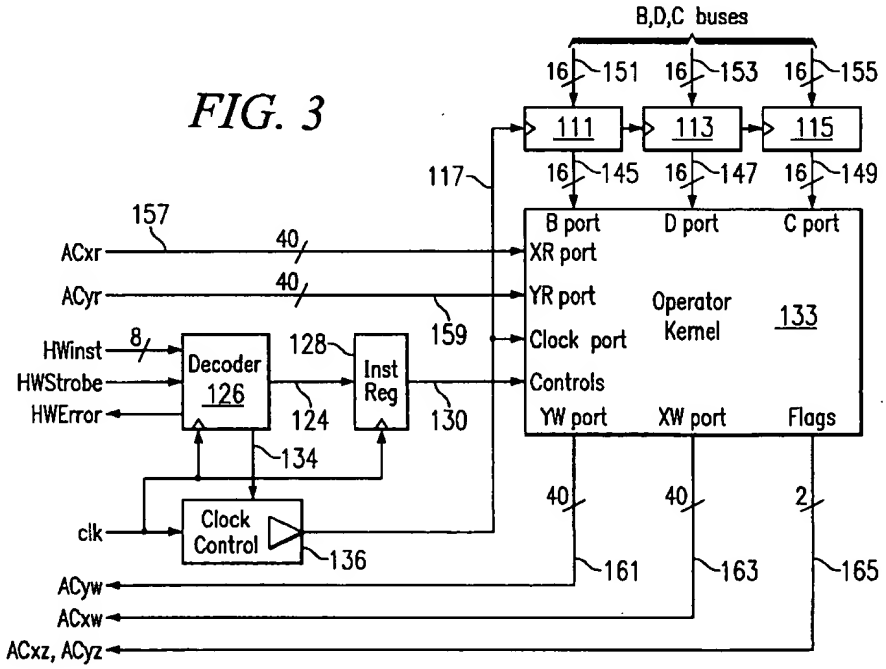

B,D,C buses
16
151
16
153
16
155
111
113
115
117
16
145
16
147
16
149
B port
D port
C port
157
ACxr
40
XR port
ACyr
40
YR port
Operator
Kernel
133
159
Clock port
HWinst
8
Decoder
126
128
Inst
Reg
Controls
HWStrobe
HWError
124
130
YW port
XW port
Flags
134
40
40
2
clk
Clock
Control
136
161
163
165
ACyw
ACxw
ACxz, ACyz

FIG. 4

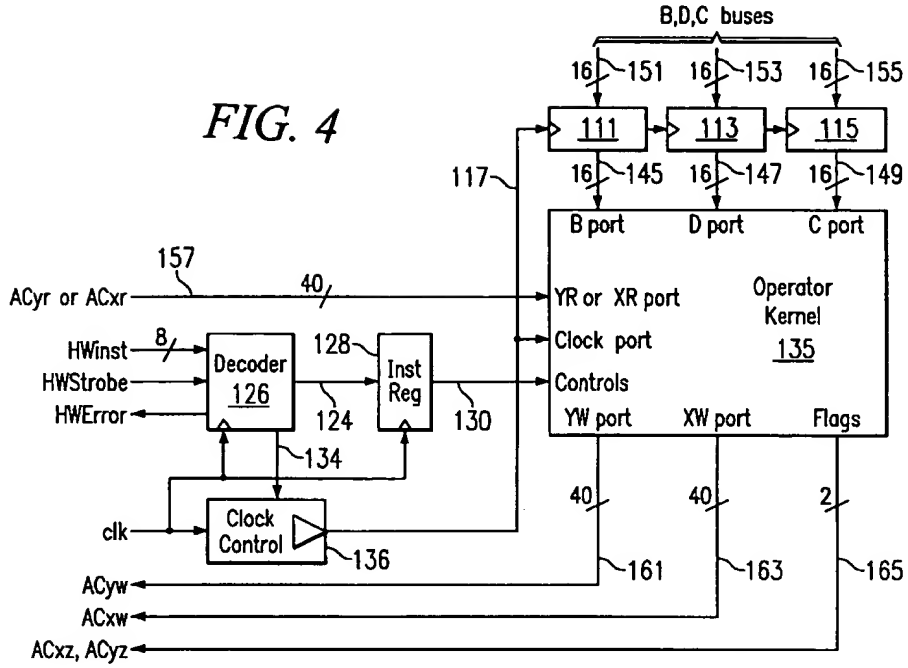


FIG. 5

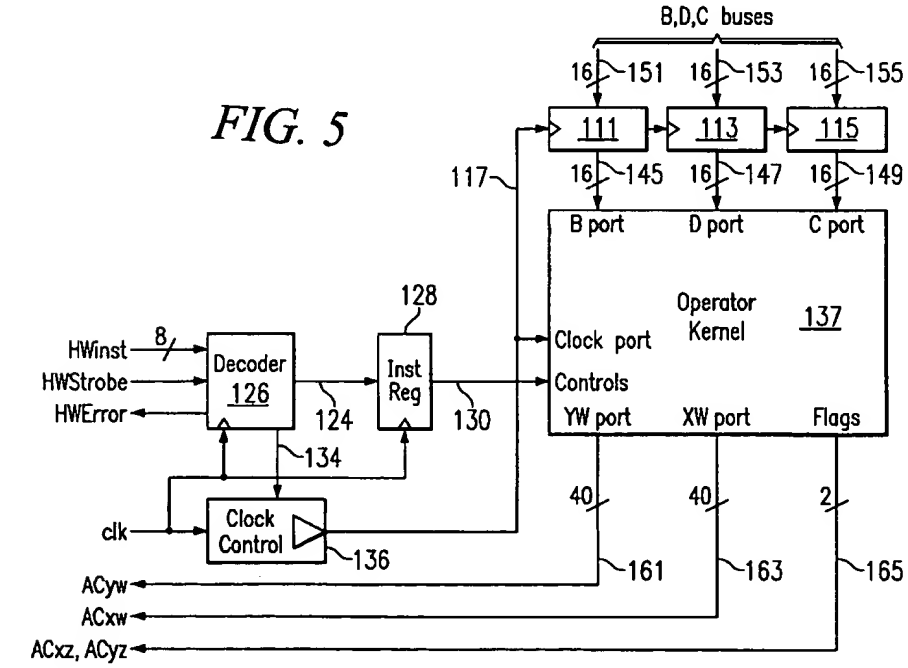


FIG. 6

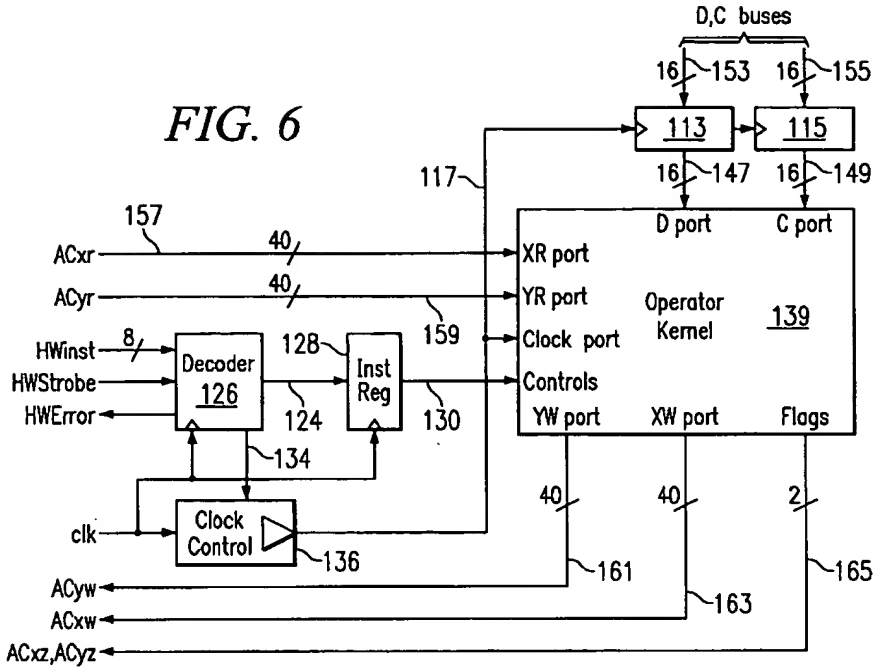

D,C buses
16
153
16
155
113
115
16
147
16
149
117
157
ACxr
40
ACyr
40
159
D port
C port
XR port
YR port
Clock port
Controls
Operator Kernel
139
HWinst
8
HWStrobe
HWError
Decoder 126
128
Inst Reg
124
130
134
YW port
XW port
Flags
40
40
2
clk
Clock Control
136
161
163
165
ACyw
ACxw
ACxz,ACyz

FIG. 7

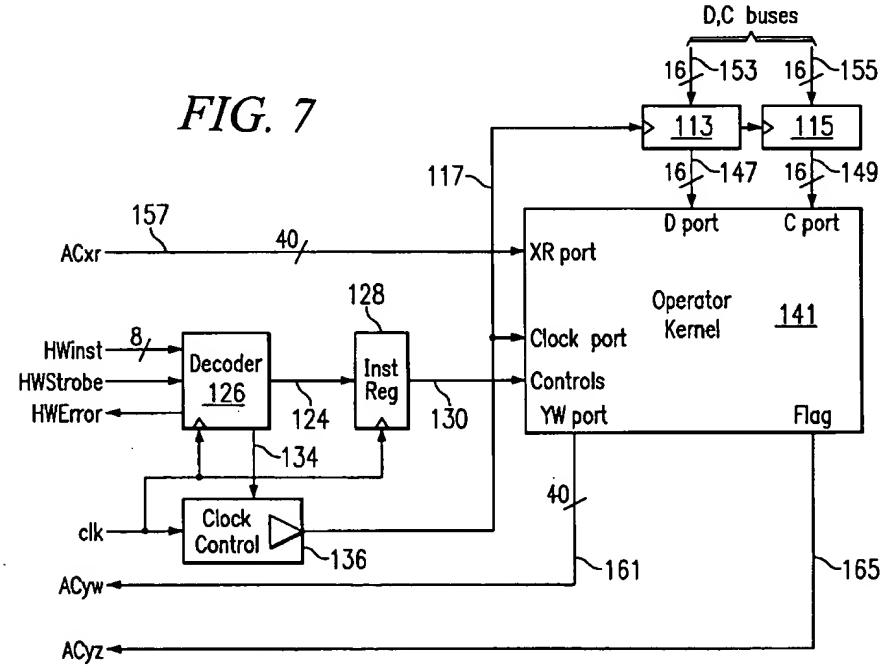

D,C buses
16
153
16
155
113
115
16
147
16
149
117
157
ACxr
40
D port
C port
XR port
128
Operator Kernel
141
HWinst
8
HWStrobe
HWError
Decoder 126
Inst Reg
124
130
Clock port
Controls
YW port
Flag
134
40
clk
Clock Control
136
161
165
ACyw
ACyz

FIG. 8

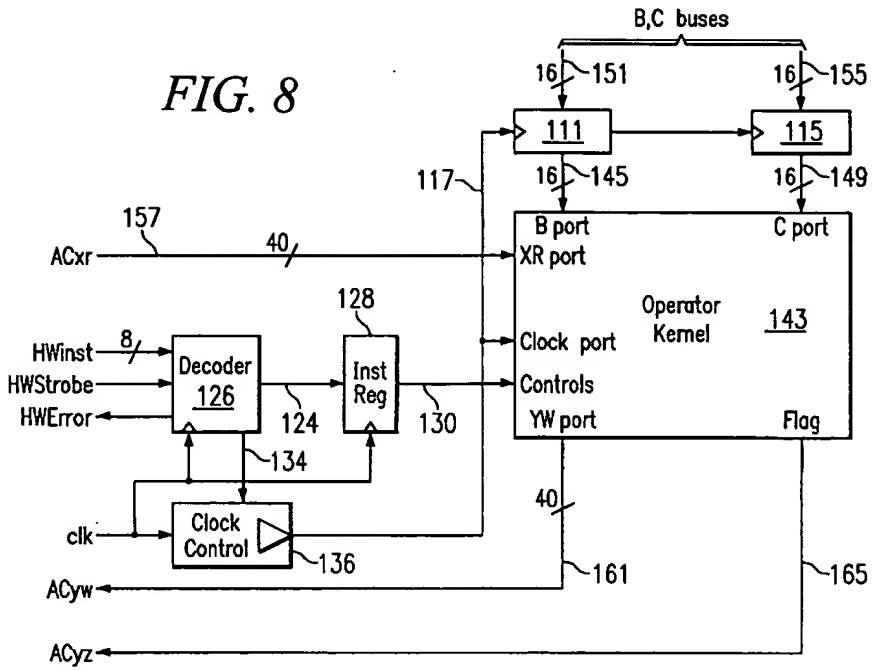

B,C buses
16
151
16
155
111
115
117
16
145
16
149
157
ACxr
40
B port
C port
XR port
128
Operator
Kernel
143
HWinst
8
Decoder
126
Inst
Reg
Clock port
HWStrobe
Controls
HWError
124
130
YW port
Flag
134
40
clk
Clock
Control
136
161
165
ACyw
ACyz

FIG. 9

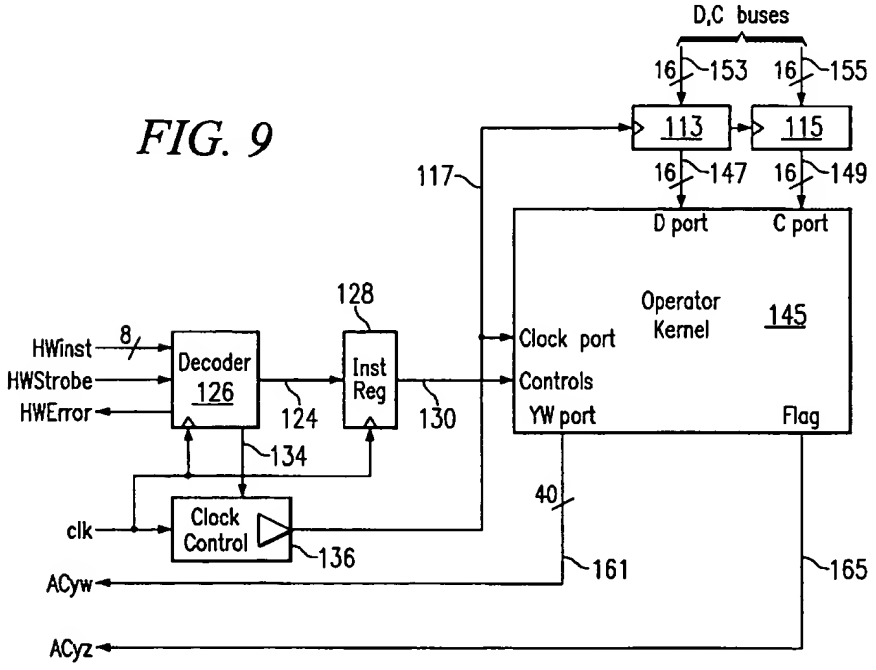

D,C buses
16
153
16
155
113
115
117
16
147
16
149
D port
C port
128
Operator
Kernel
145
HWinst
8
Decoder
126
Inst
Reg
Clock port
HWStrobe
Controls
HWError
124
130
YW port
Flag
134
40
clk
Clock
Control
136
161
165
ACyw
ACyz

FIG. 10

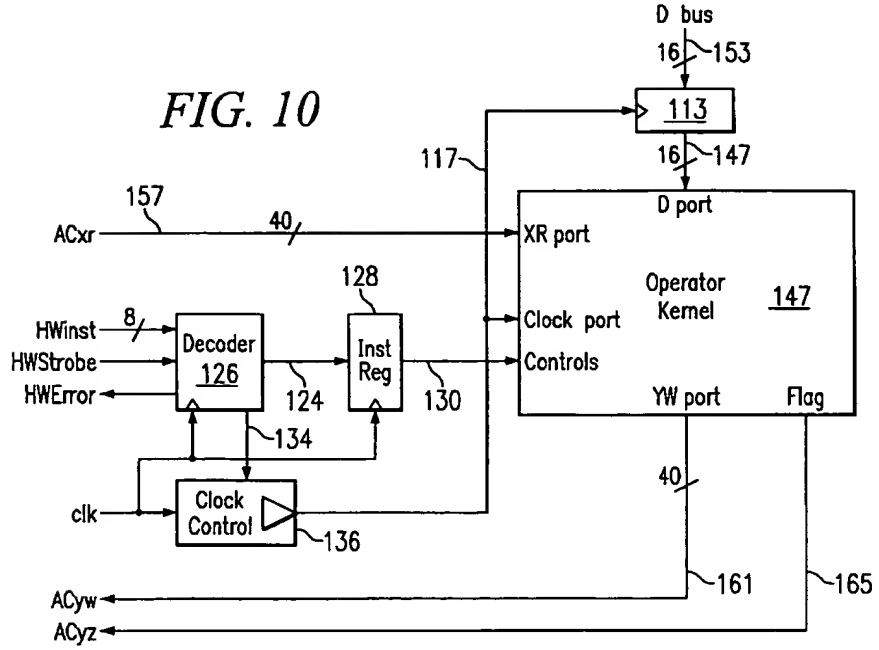

D bus
16
153
113
16
147
117
157
ACxr
40
D port
XR port
128
Operator
Kernel
147
HWinst
8
Decoder
126
Inst
Reg
Clock port
Controls
HWStrobe
HWError
124
130
YW port
Flag
134
40
clk
Clock
Control
136
161
165
ACyw
ACyz

FIG. 11

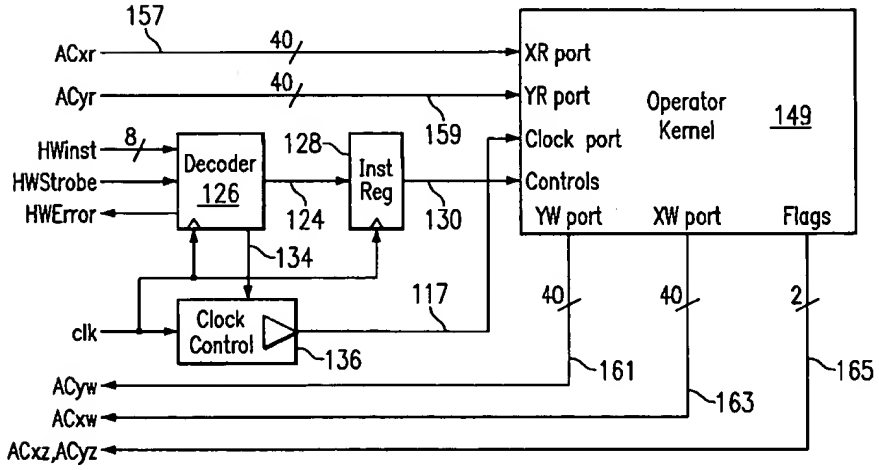
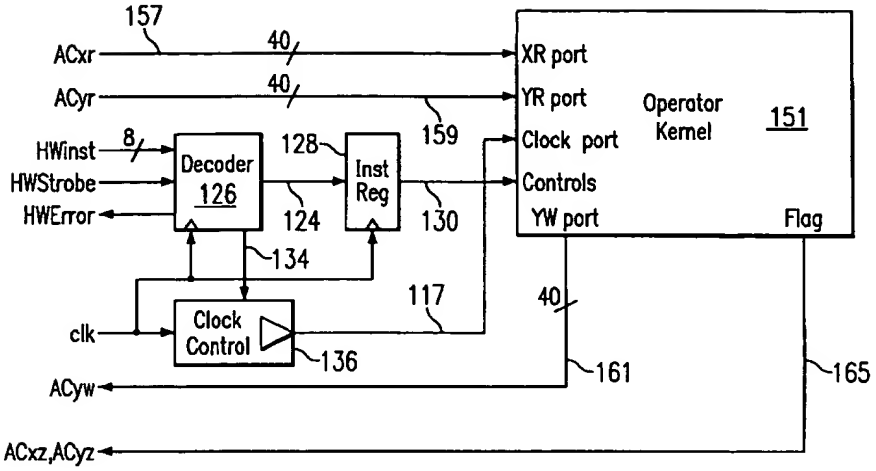

157
ACxr
40
XR port
ACyr
40
YR port
159
Operator
Kernel
149
HWinst
8
Decoder
126
128
Inst
Reg
Clock port
Controls
HWStrobe
HWError
124
130
YW port
XW port
Flags
134
117
40
40
2
clk
Clock
Control
136
161
165
ACyw
163
ACxw
ACxz,ACyz

FIG. 12



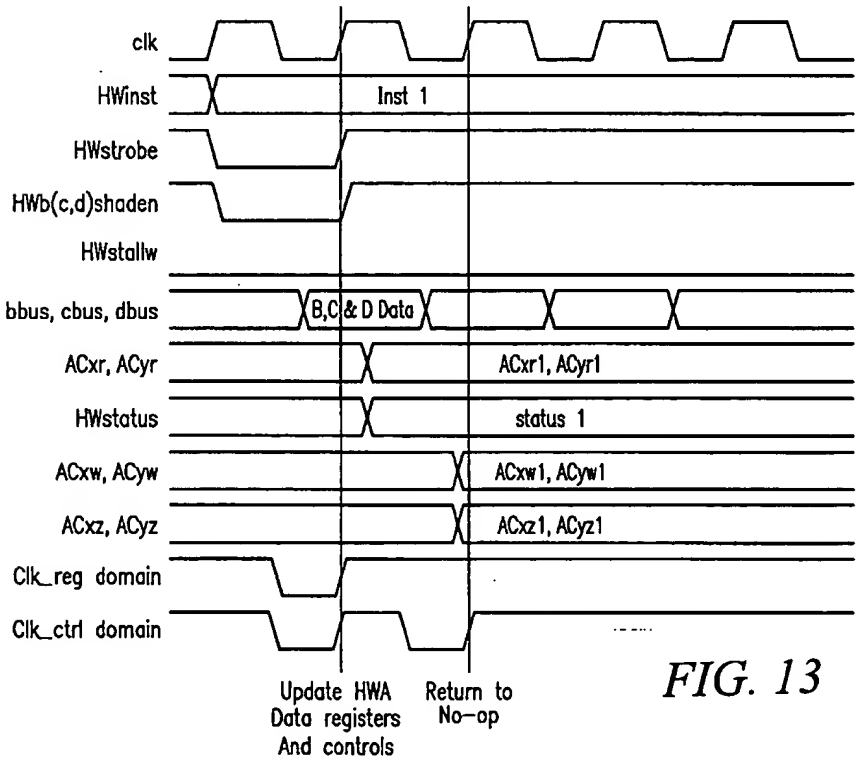


FIG. 13

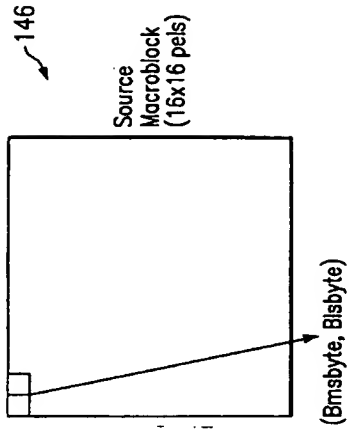


FIG. 15

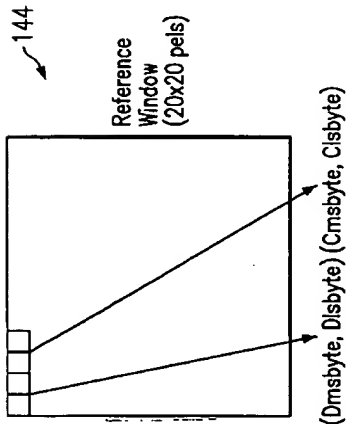


FIG. 14

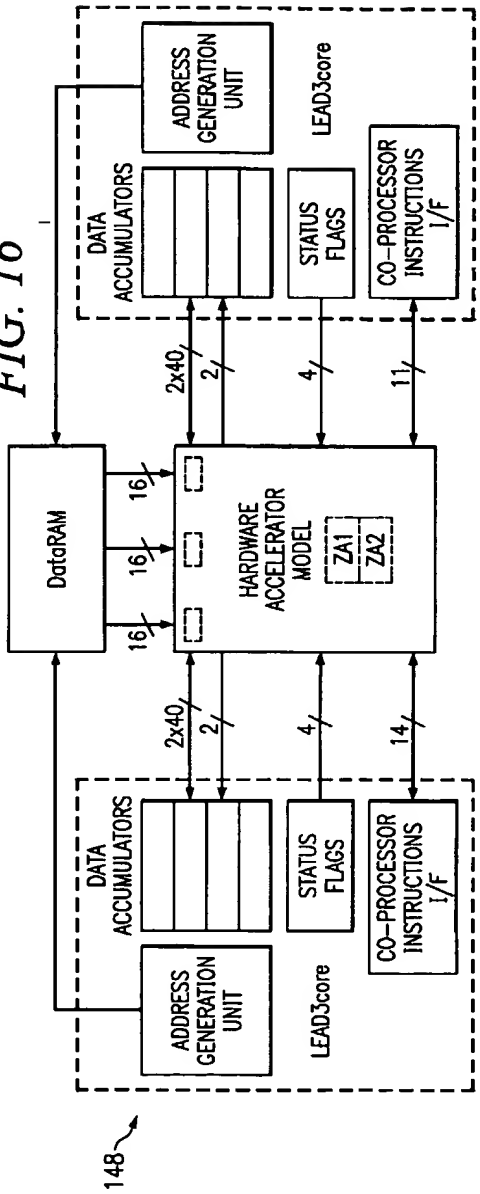


FIG. 16

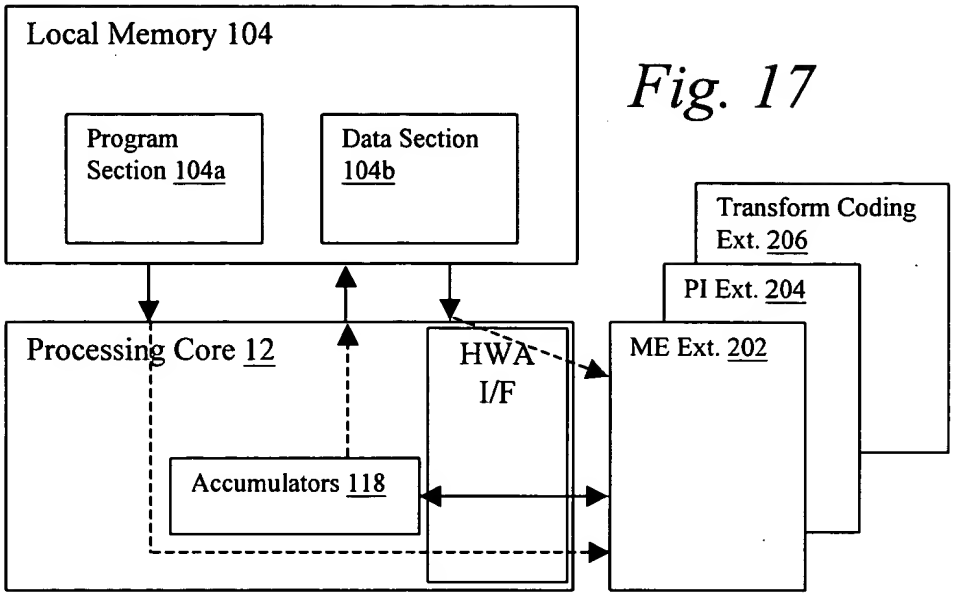
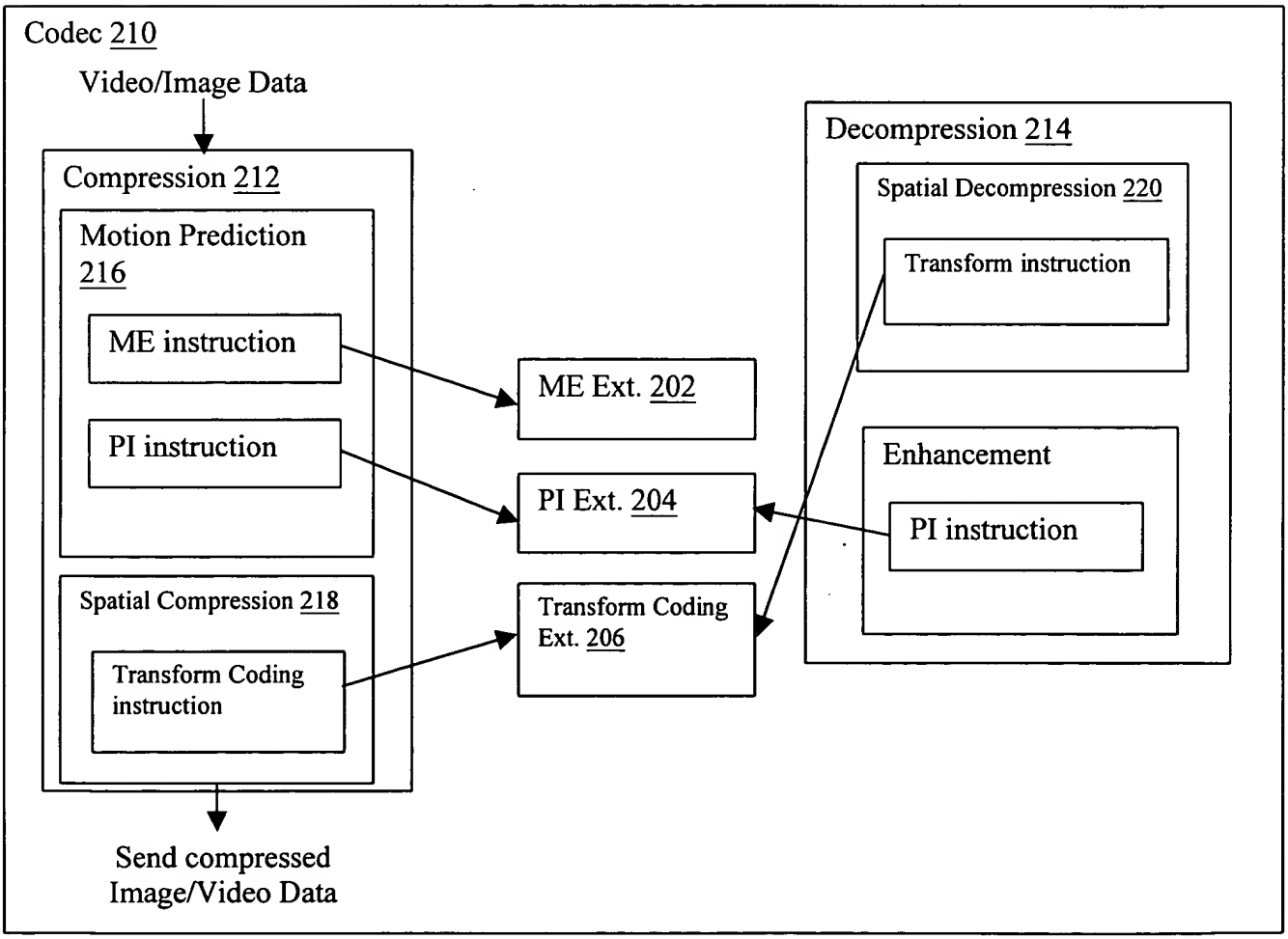


Fig. 17

Fig. 18



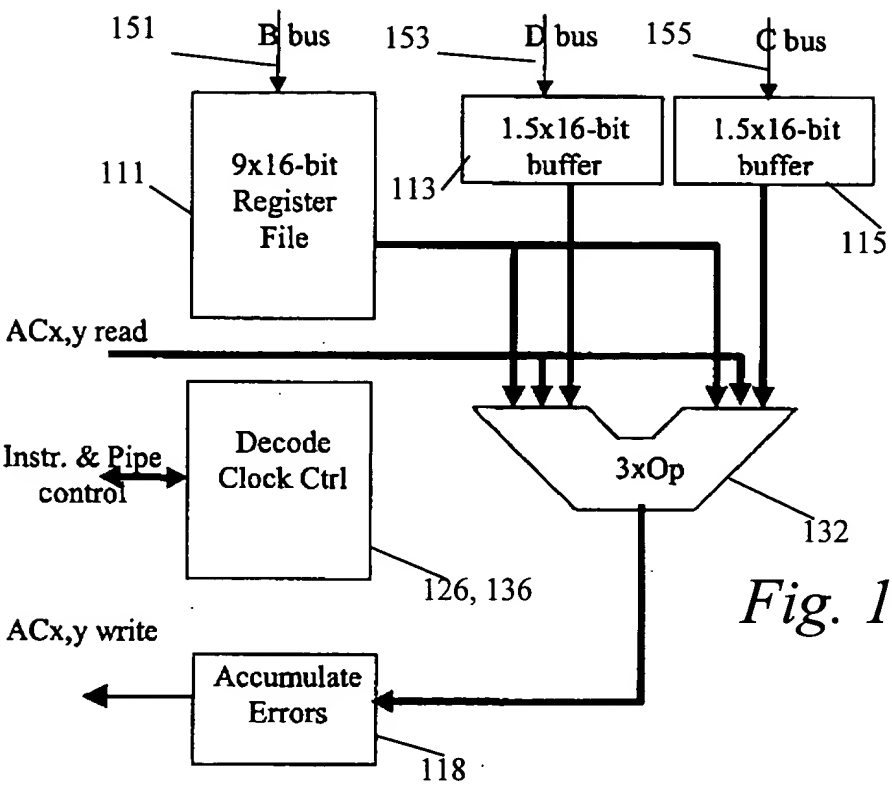


Fig. 19

Fig. 20

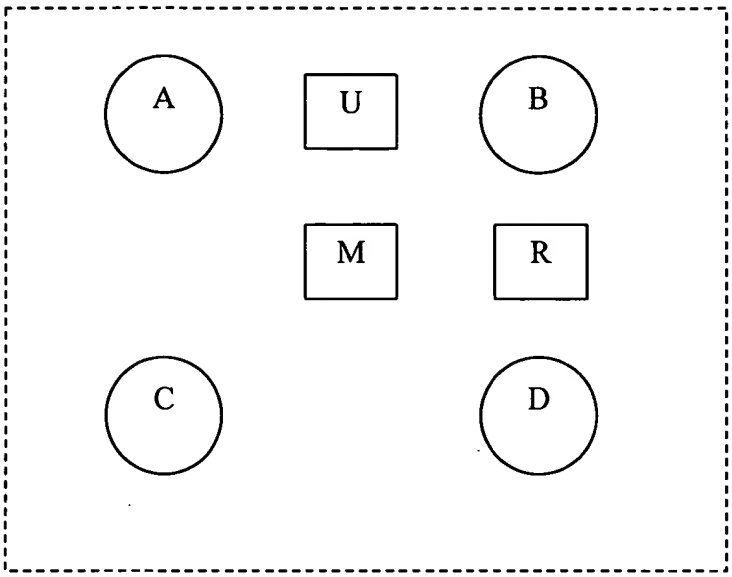
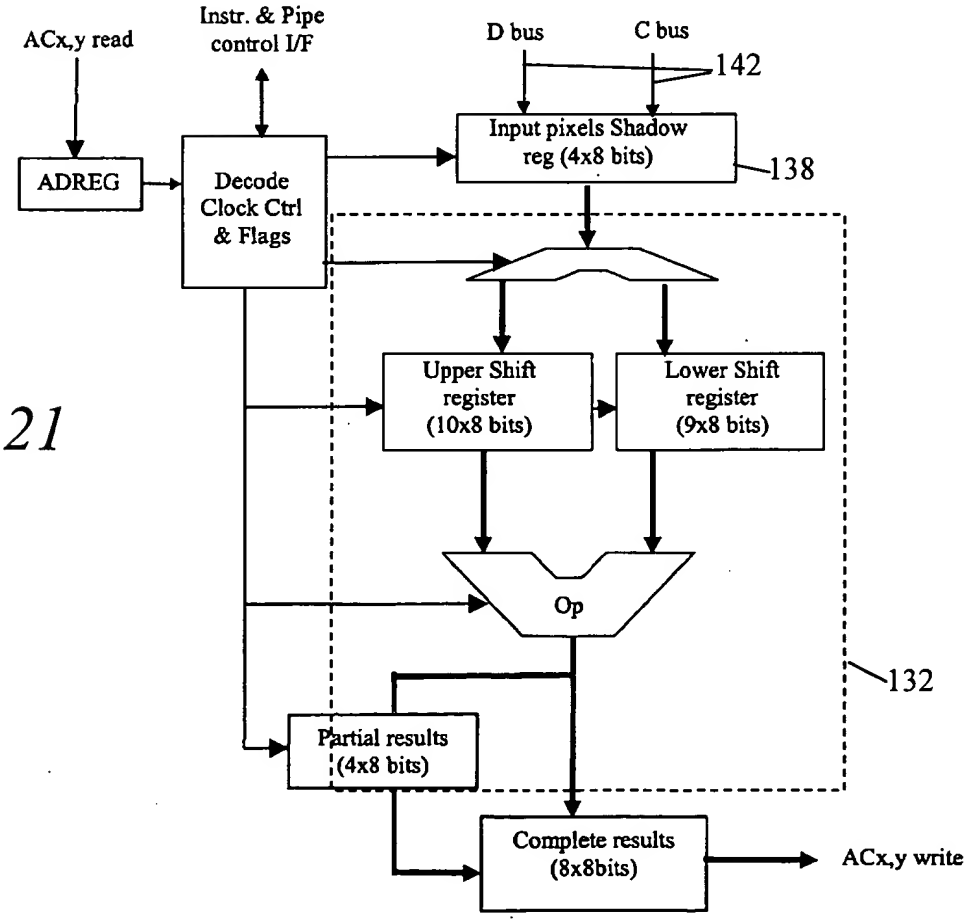

A
U
B
M
R
C
D

Fig. 21


ACx,y read
Instr. & Pipe control I/F
D bus
C bus
142
Input pixels Shadow reg (4x8 bits)
138
ADREG
Decode Clock Ctrl & Flags
Upper Shift register (10x8 bits)
Lower Shift register (9x8 bits)
Op
132
Partial results (4x8 bits)
Complete results (8x8bits)
ACx,y write

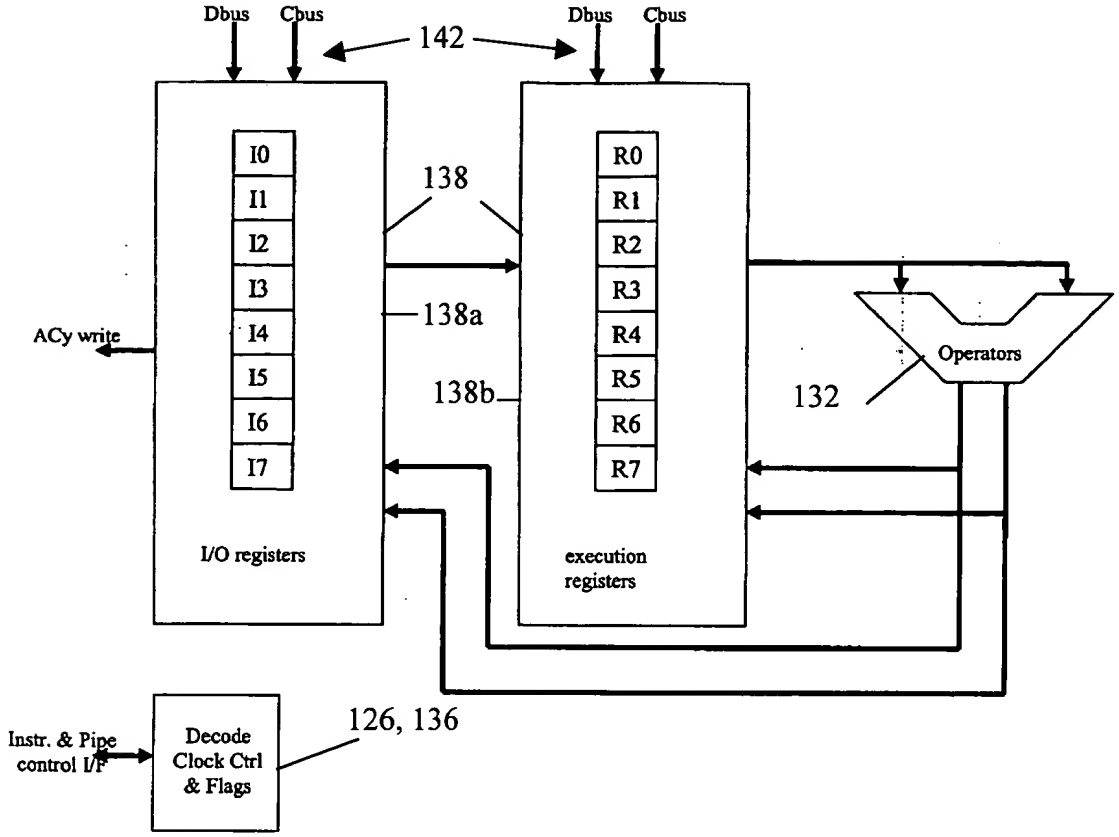


Fig. 22

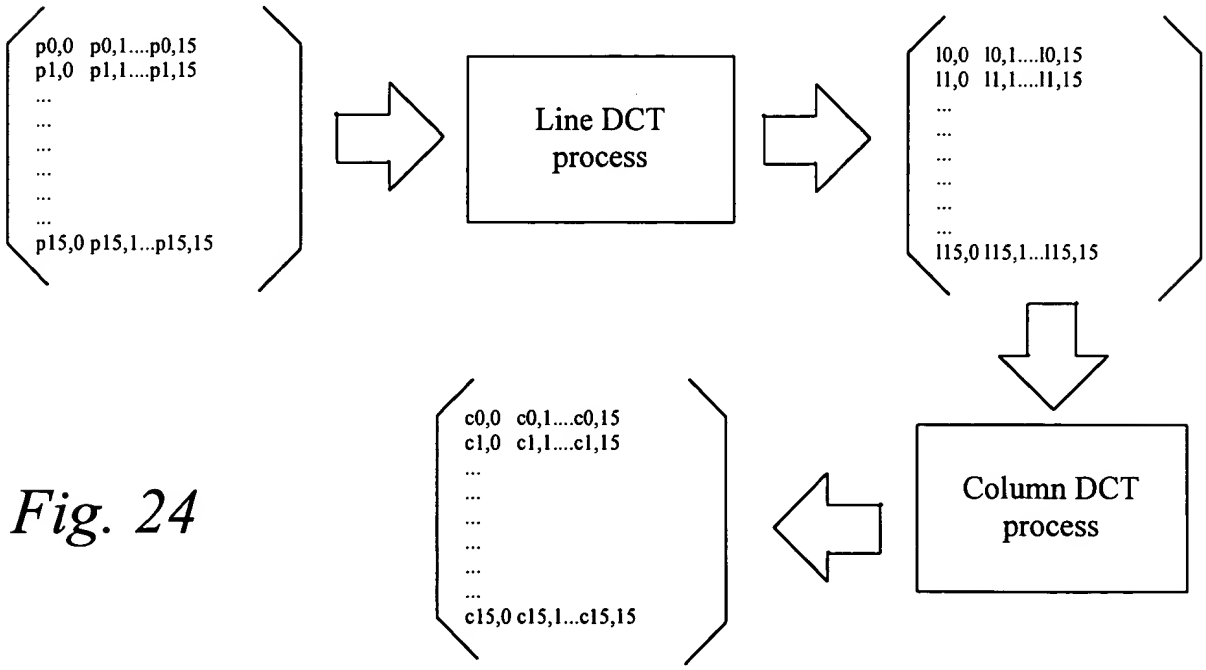


Fig. 24

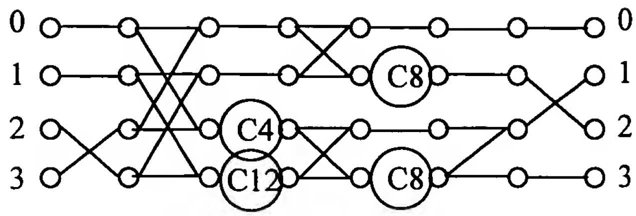


Fig. 23a

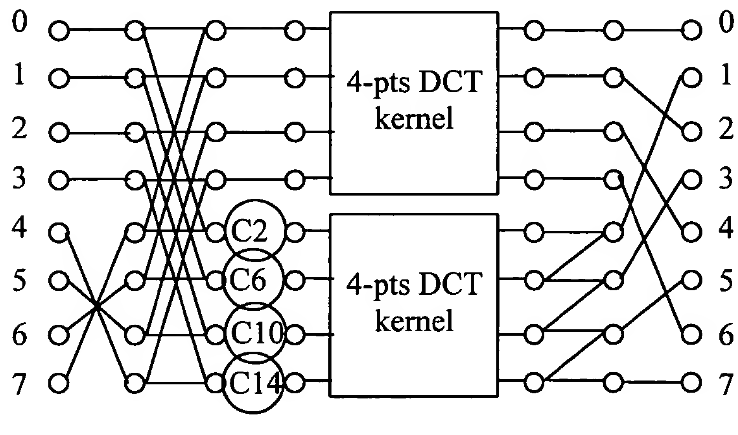


Fig. 23b

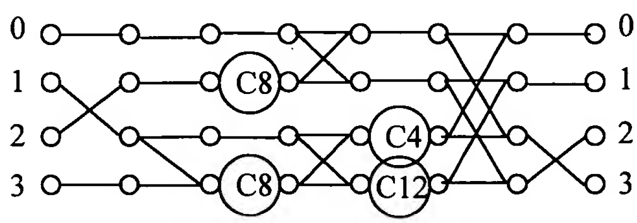


Fig. 23c

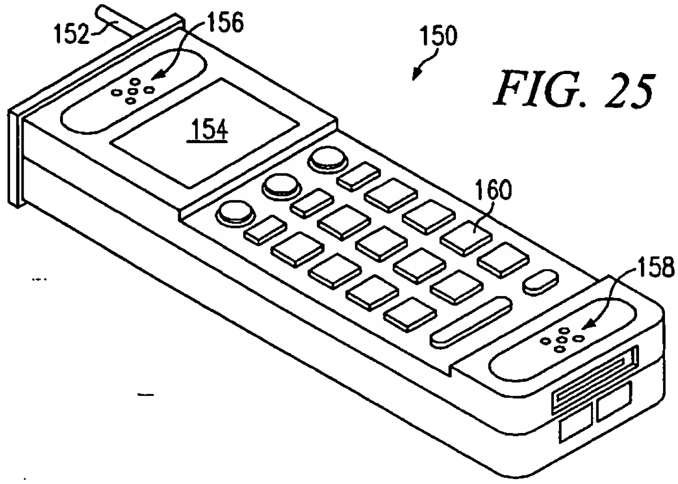

152
156
150
154
160
158

FIG. 25

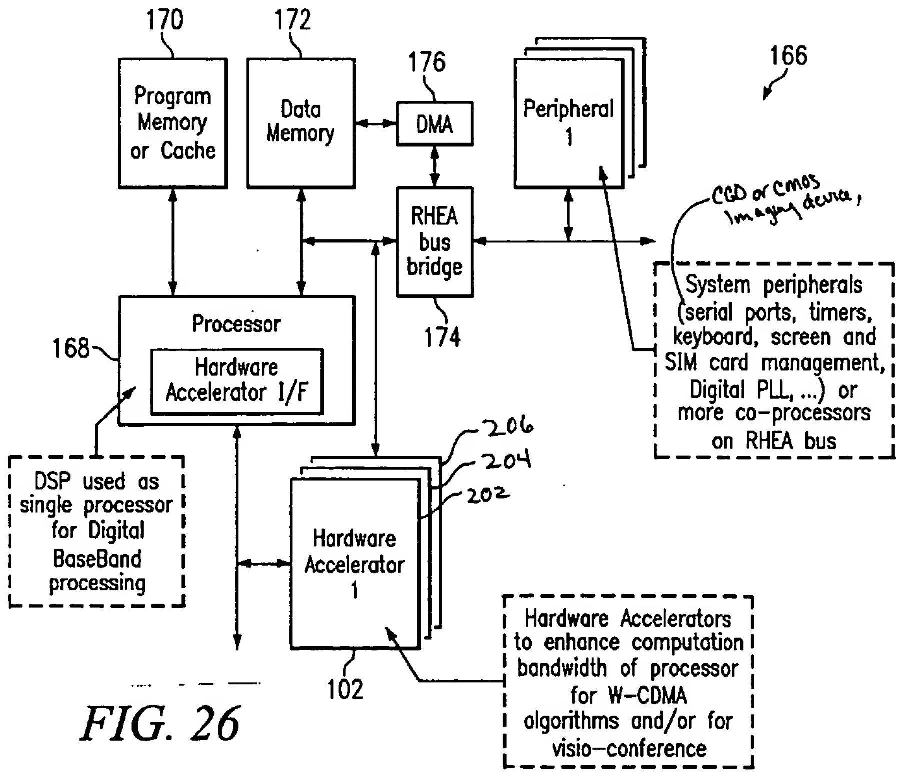

170
172
176
166
Program Memory or Cache
Data Memory
DMA
Peripheral 1
RHEA bus bridge
CCD or CMOS Imaging device,
System peripherals (serial ports, timers, keyboard, screen and SIM card management, Digital PLL, ...) or more co-processors on RHEA bus
174
168
Processor
Hardware Accelerator I/F
206
204
202
DSP used as single processor for Digital BaseBand processing
Hardware Accelerator 1
Hardware Accelerators to enhance computation bandwidth of processor for W-CDMA algorithms and/or for visio-conference
102

FIG. 26